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ABSTRACT OF THE DISCLOSURE

For a plurality of digital video signals whose frame frequencies are different, a pixel number converting circuit to convert the number of pixels is provided so that differences of the frame frequencies are replaced to differences of the numbers of pixels and a plurality of digital video signals whose frame frequencies are different can be processed by a common clock frequency. The frame frequency is detected by a frame frequency value decoder and the number of pixels in the horizontal direction of the pixel number converting circuit is properly set in accordance with the frame frequency. As mentioned above, if the differences of the frame frequencies are replaced to the differences of the numbers of pixels and the images are converted into the image in which the frame frequencies are the same and the numbers of pixels are different, the frame frequencies are equalized and the signals can be processed by the same clock.